UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,042	09/09/2003	Micha Gutman	TSL-124	3274

22888 7590 05/04/2005

BEVER HOFFMAN & HARMS, LLP
TRI-VALLEY OFFICE
1432 CONCANNON BLVD., BLDG. G
LIVERMORE, CA 94550

EXAMINER	
LINDSAY JR, WALTER LEE	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/659,042	GUTMAN ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *1-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-16 and 21* is/are rejected.

7)☒ Claim(s) *17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Election filed on 2/17/2005.

Currently, claims 1-21 are pending. Claims 1-6 have been withdrawn.

Election/Restrictions

1. Applicant's election without traverse of claims 7-21 in the reply filed on 2/17/2005 is acknowledged.

2. Claims 1-6 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected device, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 2/17/2005.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "Charge trapping region (21) and Charge trapping region (22)". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 7-8, 10, 12-13, 15 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim (U.S. Patent No. 6,765,259 filed 8/28/2002).

Kim shows the method as claimed in Figs. 6-18 and corresponding text as: forming an oxide-nitride-oxide (ONO) layer (801, 802 and 803) over a surface of a semiconductor region (401) (col. 7, lines 28-58); patterning the ONO layer to create a first set of ONO structures (Fig. 11) that define location for a plurality of diffusion bit lines of the fieldless array (col. 7, lines 28-58); forming a plurality of word lines (901) over the first set of ONO structures (Fig. 6) (col. 5, lines 1-10); and patterning the first set of ONO structures, thereby creating a second set of ONO structures, (10B) (col. 7, lines 20-27) wherein the second set of ONO structures are located entirely under the

plurality of word lines (Fig. 12) (col. 7, line 59-col. 8, line 6) (claim 7). Kim teaches that dielectric sidewall spacers (1301-1302) are formed adjacent to the word lines (Fig. 13) (col. 8, lines 18-34) (claim 8). Kim teaches that diffusion bit lines (1401-1402) are implanted through the first set of ONO structures (col. 8, lines 35-45) (claim 10). Kim teaches that the diffusion bit lines extend along a first axis, and the word lines extend along a second axis, perpendicular to the first axis (col. 8, lines 19-45) (claim 12). Kim teaches depositing a layer of polysilicon (901) over the first set of ONO structures; forming a photoresist mask (1001) over the layer of polysilicon; etching the layer of polysilicon through the photoresist mask; and etching the first set of ONO structures through the photoresist mask (col. 7, lines 19-58) (claim 13). Kim teaches the step of etching the first set of ONO structures is implemented by a series of wet etches (col. 7, lines 36-58) (claim 15). Kim teaches the step of etching the first set of ONO structures results in the removal of portions of the ONO structure under the layer of polysilicon (col. 7, lines 19-58) (claim 21).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claim 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (U.S. Patent No. 6,765,259 filed 8/28/2002) in view of Applicants' Admitted Prior Art (US Application 10/659,042, filed 9/9/2003).

Kim shows the method substantially as claimed and as described in the preceding paragraphs.

Kim lacks anticipation only in not explicitly teaching that: 1) a gap-filling oxide is formed between the word lines (claim 9); and 2) thermally growing bit line oxide regions are formed over the diffusion bit lines (claim 11).

AAPA shows a fieldless array. In paragraph [0006], Fig. 4b, dashed lines 193 and 194 corresponding to the gap filling oxide associated with polycide word. It should also be noted that thermally grown oxides are well known in the art. This is done to ensure relatively high density devices.

It would be obvious to one of ordinary skill in the art, at the time the invention was made to modify the method of Kim, by forming gap-filling oxide between the word lines, thermally growing bit line oxide regions over diffusion bit lines, as taught by AAPA, with the motivation that the process help to ensure relatively high density devices.

10. Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (U.S. Patent No. 6,765,259 filed 8/28/2002) in view of Nachumovsky (U.S. Patent No. 6,174,758 dated 1/16/2001).

Kim shows the method substantially as claimed and as described in the preceding paragraphs.

Kim lacks anticipation only in not explicitly teaching that: 1) the steps of etching the layer of polysilicon and the first set of ONO structures are implemented by a reactive ion etch (RIE) (claim 14); and 2) the step of etching the first set of ONO structures is implemented by a wet etch and a dry/reactive ion etch (RIE) (claim 16).

Nachumovsky shows a semiconductor chip having a fieldless array there on. The ONO (463, 462 and 461) layer goes through a series of etches. One such etch process is a first wet etch, followed by a dry etch for example an (RIE) etch (col. 7, lines 34-40). It would therefore be desirable to have an efficient process for fabricating high and low voltage CMOS logic transistors and fieldless array transistors on the same wafer (col. 1, lines 48-56).

It would be obvious to one of ordinary skill in the art, at the time the invention was made to modify the method of Kim, by using an RIE etch to pattern the ONO structure and a combination of wet etch and RIE etch to pattern the ONO structure, as taught by Nachumovsky, with the motivation that Nachumovsky teaches that it is desirable to have an efficient process for fabricating high low voltage CMOS logic transistors and fieldless array transistors on the same wafer.

Allowable Subject Matter

11. Claims 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...wherein the step of etching the first set of ONO structures is extended to etch the semiconductor substrate to a depth of 50 to 400 Angstroms, as required by claim 17;

...depositing a thin dielectric spacer having a thickness up to about 400 Angstroms over the etched layer of polysilicon; and then

etching back the thin dielectric spacer layer, prior to etching the first set of ONO structures, as required by claim 18;

...further comprising performing a re-oxidation step after the step of etching the first set of ONO structures, as required by claim 19;

...wherein the re-oxidation step results in the formation of about 20-200 Angstroms of silicon oxide, as required by claim 20.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
April 20, 2005